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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,311	03/18/2004	Shawn D. Rogers	10599/131	5776

7590 06/20/2006

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EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,311	ROGERS ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *23-60* is/are withdrawn from consideration.

5)☒ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-7 and 12-22* is/are rejected.

7)☐ Claim(s) *9-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 pgs*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 23-60 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/17/06. Claims 1-10 and 12-22 (claim 11 was missing, see paragraph 2 below for renumbering the claims) are considered in this Office Action.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 12-22 have been renumbered 11-21.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 7 and 13-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Libous et al. (US 20040183184).

Regarding claim 1, as shown in figures 1-2, 4-5 and 7-6, Libous discloses a multilayer board 10 (chip package, paragraph 19) comprising:

(a) A central area 16 (a square center cutout, par. 19) on a first layer 50 (dielectric layer, par. 19) in which an electrical device 18 (a chip, par. 19) is to be mounted;

(b) a localized array of elements 36/22 (metallic conductor and metal pads, par. 19 and 21; also see figures 4-5, par. 24-31) at least partially surrounding the central area 16 on the first layer.

Regarding claim 2, as shown in figures 1-2, Libous discloses the elements comprise capacitors formed on the first layer. It is noticed that, beside the capacitance formed by the ground layer 12 and the power layers 62/63, the pad 22 (ground connected) is surrounded by power layers 62/63 thus inherently function as a capacitor. It is further noticed that the layer 50 is a high-K dielectric layer. Furthermore, for the same point of view and as shown in figure 6 and paragraphs 32-36, capacitance is inherently formed in the clearance hole 137 having ground conductor 116 formed within and being surrounded by power layer 113; hence each clearance hole is considered to function as a capacitor.

Regarding claim 3, Libous discloses the elements comprising conductive coplanar patches 22 (metal pads, para. 19) formed on a second layer (considering the top layer of multilayer 26, see par. 20).

Regarding claim 7, Libous discloses the patches that are disposed adjacent to a signal line (formed in substrate 26), which disposed on the second layer (considering

on the opposite surface where pads 22 are formed). It is noticed that substrate 26, which comprises a multiple layers having circuitized copper foil for signal lines, see paragraph 20.

Regarding claim 8, Libous discloses a characteristic (distances from center) of the patches in the array changes with distance from the center.

Regarding claims 13-14, as shown in figure 1, Libous further discloses a ground plane 74 (par. 21) to which the patches 22 are connected through multiple conductive rods 72 (ground vias, par. 21).

Regarding claim 15, Libous discloses the elements comprising conductive coplanar patches 22 formed on the second layer.

Regarding claim 16, as clearly shown in figures 1-2 and 4-5, Libous discloses the array, which completely surrounds the central area.

Regarding claim 17, as shown in figures 4-5, Libous discloses the number of elements in the array in the particular direction from the central area being different from the number of elements in the array in at least one direction orthogonal or parallel to the particular direction from the central area.

Regarding claim 18, Libous discloses the elements inherently having the same characteristics throughout the array.

Regarding claim 19, as shown in figure 5, Libous discloses multiple arrays that are present in the same layer (considering any small group of the elements as an array; in other words, a large array comprises a multiple sub-arrays).

Regarding claim 20, as shown in figure 2, Libous discloses 2 elements that are in the array in the particular direction.

Regarding claim 21, Libous discloses the conductive rods 72 that are plated through holes (see para. 4).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 4-6 and 11-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Libous in view of Smith (US 6538313).

Regarding claim 4, Libous discloses every limitation as shown in claim 3 above, but does not disclose a C-plane formed in the central area.

It is old and known in the art that capacitors are frequently used to suppress unwanted noise (bypass capacitor) or to provide a stable supply of power to a circuit. In the case of bypassing capacitors, capacitors are generally placed as close as practical

to a die load in order to increase the capacitors effectiveness. The bypassing capacitors are mostly mounted to the die side (surface mounting capacitors), land side (capacitors are mounted on opposite surface where the die being mounted), or embedded within a substrate right underneath the die (a C-plane).

Smith, as shown in figures 3A-3B, discloses an integrated circuit package 100 comprising an embedded capacitor structure formed underneath a die. The structure comprises a capacitor 121 formed underneath a die 120. The capacitor is formed by sandwiching a dielectric material 380 between a die attach plate 308 and a substrate plate 107, see column 2, line 54 continuing column 3, line 8.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teaching(s) from Smith about the capacitor 121 formed underneath a die on the board 10 of Libous, thus producing a C-plane in the central area underneath the semiconductor chip 18 in order to suppress unwanted noise generating from the chip.

Regarding claims 5-6, Libous in view of Smith, discloses the C-plane, which is coplanar with the patches (because the capacitor must be formed in the substrate 26 and must be near the chip 18 for the capacitor effectiveness), and the C-plane is also formed on a third layer extending in parallel with the first and second layers (the C-Plane contains at least 3 layers).

Regarding claims 11-12, Libous disclose every limitation as shown in claim 3 above, but fails to disclose the patches having rectangular shapes and the patches are larger than the electronic device and extended throughout the central area.

As discussed in claim 4 above, Libous in view of Smith, discloses the shape of the patches (a capacitor plate underneath the chip, see Smith, figures 1A-3B) that are rectangular and larger than the electronic device and extended throughout the central area.

Allowable Subject Matter

8. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

9. The following is a statement of reasons for the indication of allowable subject matter: The prior arts fail to teach, disclose, suggest, either alone or in combination, at least on claim 8 that the characteristic of the patches in the array changes with distance from the central area, wherein the characteristic includes sizes of the patches and the shapes of the patches.

Citation of Relevant Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

McKinzie et al. (US 6690327) disclose a mechanically reconfigurable artificial magnetic conductor.

Simpkin et al. (US 6218978) disclose a frequency selective surface.

Diaz et al. (US 6512494) disclose a multi-resonant, high-impedance electromagnetic surfaces.

McKinzie (US 6476771) discloses an electrically thin multi-layer bandpass radome.

Yablonovitch et al. (US 6262495) disclose a circuit and method for eliminating surface currents on metals.

Schumacher (US 5940278) discloses a backing plate for gate arrays or the like carries auxiliary components and provides probe access to electrical test points.

Howard et al. (US 5708569) disclose an annular circuit components coupled with printed circuit board through-hole.

Bothra et al. (US 6020616) disclose an automated design of on-chip capacitive structures for suppressing inductive noise.

Li (US 6907658) disclose manufacturing methods for an electronic assembly with vertically connected capacitors.

Figueroa et al. (US 6388207) disclose an electronic assembly with trench structures and methods of manufacture.

Schaper (US 6388200) disclose an electronic interconnection medium having offset electrical mesh plane.

Figueroa et al. (US 20040022038) disclose an electronic package with back side, cavity mounted capacitors and method of fabrication therefor.

Panella et al. (US 6885563) disclose a power delivery and other systems for integrated circuits.

Okabe et al. (US 6757178) disclose electronic circuit equipment using multilayer circuit board.

McCormack et al. (US 20040207042) disclose a structure and method for embedding capacitors in z-connected multi-chip modules.

Nakamura (US 6722028) discloses a method of making electronic device.

McKinzie et al. (US 6774866) disclose a multiband artificial magnetic conductor.

Ogawa et al. (US 6577490) disclose a Wiring board.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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